2.1µm LFM Automotive Pixel with Single Photodiode and 126 dB of Single Exposure Dynamic Range

Manuel Innocent[1], Pei Heng (Benjamin) Hung[2], Grady Anderson[3], Bartosz Banachowicz[2], Harshvardhan Jog[3], Gurvinder Singh[4], Bharat Balar[4], Anirudh Oberoi[4] and Maheedhar Suryadevara[4]

onsemi, [1] Schaliënhoevedreef 20B, 2800 Mechelen, Belgium, Manuel.Innocent@onsemi.com, tel +32 15 446 390
[2] San Jose CA, USA [3] Nampa ID, USA [4] Bangalore, India

This paper reports on work in progress on a 2.1 µm rolling shutter HDR pixel for automotive applications.

We previously reported on an overflow pixel with a single exposure dynamic range (SE DR) of 110 dB and an SNR above 25 dB at each of the transition points up to 125°C [11]. This paper discusses extending the SE DR of this architecture to 126 dB (SNR1 based). To our knowledge this is the highest SE DR reported for a linear mode single PD pixel. At the pixel level the main improvement is an increase in the overflow capacitance. At the circuit level the focus is on reducing the read noise by increasing the analog gain, reducing the bandwidth and introducing correlated multiple sampling. With a second exposure the total dynamic range is up to 150 dB. This paper presents test chip results and discussion of the architectural choices.

Motivation

The most common techniques for extending the dynamic range of an image sensor are multiple exposure [1-3], split photo diode [4-6] and overflow [7-11]. Multi exposure combines images with different integration times which causes artefacts on moving objects or pulsed light sources. The case with pulsed light sources is of particular interest for automotive applications as traffic signs and taillights of cars often use pulsed LEDs. The split photo diode approach allows for a high flicker free dynamic range but does not scale well to a smaller pixel pitch and the consistency of color and MTF between the diodes is an issue. Therefore, our sensor uses overflow from a single photo diode onto a very large capacitor.

The proposed pixel can be operated with a short second exposure to reach a total DR of up to 150 DB. The first exposure has sufficient DR to capture all flickering light sources so there will not be any flickering and also motion artefacts will be limited because generally only the sun and its reflections will be in the short T2.

Philosophy

The DR of this pixel is maximized both at the low side and at the high side. The DR is extended at the low side by reducing the read noise floor which is mostly a circuit design effort while the DR is extended at the high side by maximizing the low gain overflow capacitor. The read noise floor is reduced by a combination of increasing the gain of the amplifier between the pixel and the ADC, reducing the bandwidth of the column and amplifier settling and applying correlated multiple sampling (CMS). All these changes slow down the sensor. To maximize the frame rate the number of pixel reads in the long integration time is limited to two: one PD read and one overflow read. The previous generation had two separate PD reads, one with high analog gain and one with low analog gain. The single PD read now has conditional gain. Conditional gain applies high analog gain to small signals and low analog gain to large signals.

The DR is extended at the high side by increasing the overflow capacitance. This is primarily a technology feature. However, it also requires design changes. A higher capacitance has higher kT/C noise on the overflow read, which is inevitable. It also has a higher input referred read noise due to the reduced gain. This can be compensated by increasing the analog gain in the readout path. Since also the full swing of the overflow signal must be read the overflow read also has conditional gain.

Pixel design, operation, and performance

Figure 1 shows the pixel schematic. It is an overflow pixel with an additional dual conversion gain (DCG) transistor. The DCG transistor can add capacitance to the FD. But, in this case, it is used to pump up the FD level during the transfer operation. This extends the swing on the high conversion gain read and avoids adding an additional, medium conversion gain read. So, the pixel combines overflow to a low gain capacitor with a dual gain readout. The low gain capacitor (Clg) is a trench MiM that allows for a full well charge of 2200 ke⁻ on the product.

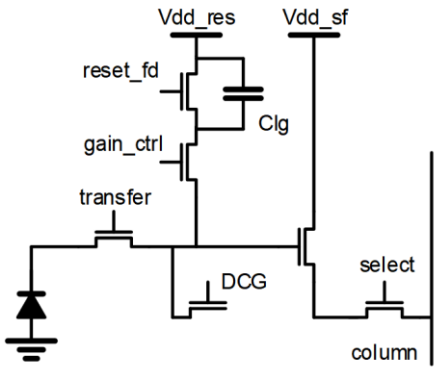

Figure 1: Schematic of the pixel. Clg is a trench MiM overflow capacitor. The dual conversion gain transistor (DCG) is used to pump up the FD level during the transfer operation.

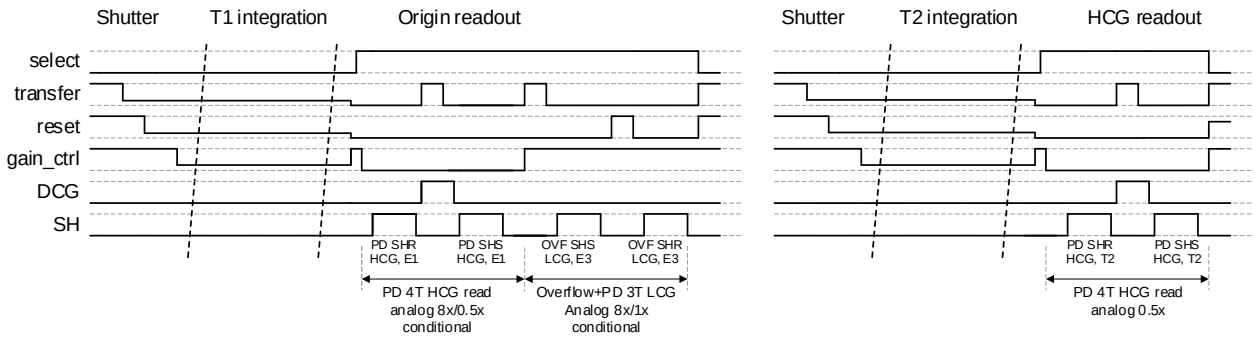

Figure 2: Timing diagram of the overflow T1 with dual gain origin mode read and PD T2 high gain read. The two reads of T1 are both read with conditional analog gain and optionally correlated multiple sampling. These additional operations in the readout path are not included in this pixel timing diagram. The overflow T1 is also referred to as a "Super-Exposure" as it combines signals from multiple in pixel readout gains and covers a very wide DR.

Figure 2 shows a simplified timing diagram for the pixel operation with a dual gain T1 read and a high gain T2 read. Both T1 reads have a response starting from the origin. Signal charge is not reset in between the reads. The low gain read contains all charge from the PD and the overflow capacitor. The high conversion gain PD reads are correlated double sampling reads while the low conversion gain overflow read is double sampling read. Both the T1 reads have conditional analog gain and optionally correlated multiple sampling.

Figure 3 shows the measured SNR for multiple temperatures on the test chip with overflow FW of 2100 ke$^-$. This TC has a SE DR of 124 dB at room temperature. Another instance of the test chip has a larger capacitor with an overflow FW of 2700 ke$^-$ which has a SE DR of 126 dB at room temperature. On the product the capacitor is limited to a FW of 2200 ke$^-$ to maintain the transition SNRt at the HCG to LCG transition at 25dB so figure 3 is fairly representative for the product. The SNRt on the HCG to LCG transition stays above 27 dB up to 100°C. At 125 °C the SNRt still maintains a level around 25 dB.

The SNRt at the transition between the T1 overflow read and T2 is not shown in this figure. It does not change significantly with temperature. It is mainly a function of the integration time ratio. This ratio can be chosen at runtime and trades SNRt for total DR. With focus on higher DR e.g. a ratio of 5000 results in an SNRt of 26 dB and a total DR of 150 dB. By giving up some DR the SNRt can be improved significantly e.g. a ratio of 2000 results in an SNRt of 30 dB and a total DR of 143 dB.

These SNR curves illustrate that this pixel is designed for high temperature operation. The performance at 60 °C and 80 °C is almost indistinguishable and at 100 °C there is only a minor degradation of SNR1. At 125 °C the SNR1 degrades noticeable due to increased PD DSNU but is on par with our same pixel size multi-exposure sensor which is state of the art and has a much simpler pixel operation. Also, the SNRt is hardly changing with temperature up to 100 °C since it is read noise dominated. Only at 125 °C FD DSNU dominates over the read noise.

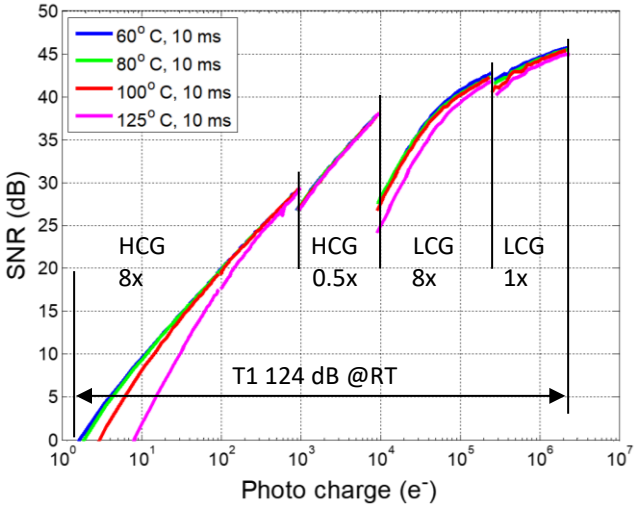

Figure 3: Measured SNR of the test chip as a function of exposure at 10 ms integration time. The data is from four separate measurements each plotted in their relevant range. The HCG 0.5x read is a DS read on the TC while it will be a CDS read on the product. On the product the HCG 8x to 0.5x transition will be almost invisible.

Overflow capacitance trade-off

The DR of this pixel is maximized by increasing the low gain capacitance. However, increasing the capacitance increases the noise, so there is a trade-off between DR and SNRt at the HCG to LCG transition. Increasing the capacitance increases the noise through two mechanisms: it increases the kT/C noise, and it increases the input referred read noise because of the reduced charge to voltage conversion gain. The increased kT/C noise is fundamental so it will eventually limit the usable capacitance. kT/C noise can only be eliminated by changing the LCG (3T) readout to CDS. This requires an external memory to store the reset value which is practically infeasible for a low-cost product. The increased input referred read noise can be compensated to some extent by reducing the noise of the analog readout path, which is commonly achieved by increasing the analog gain.

Pushing the HCG to LCG transition point to higher signal would allow for more noise in the LCG read, but the transition point is fixed at 10 ke⁻ because of other design decisions. The PD readout is limited to one read for speed reasons. This implies a trade off between FW and read noise since the pixel output swing is limited. The high conversion gain is maximized given a source follower size that is required to meet the speed. With the maximized conversion gain and the maximized pixel output swing the linear FW of the PD read is limited to 10 ke⁻. To achieve this large pixel swing without charge sharing the FD is pumped to a higher voltage during the transfer using the DCG device. The full pixel output swing is read with 0.5x attenuation in the amplifier as it exceeds the ADC input swing. Pushing the transition to higher signal would either increase noise by reducing the conversion gain or reduce speed by adding a medium gain read.

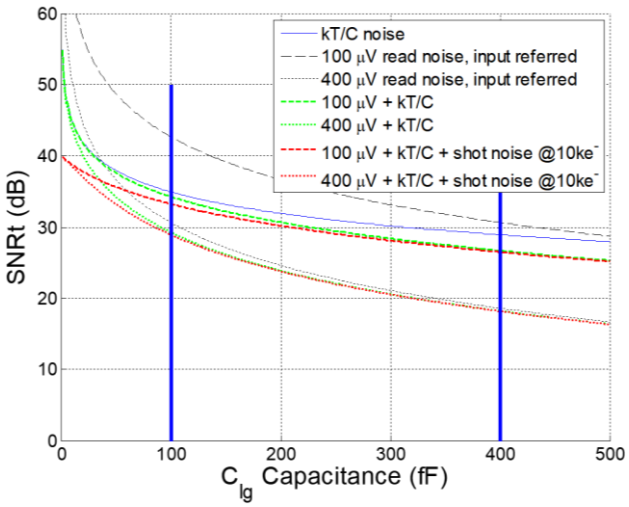

Figure 4: SNRt of the LCG read at the HCG-LCG transition (@10 ke⁻) as a function of low gain capacitance for readout path noises of 100 and 400 µV.

Figure 4 shows the SNRt at the HCG to LCG transition at 10 ke⁻ as a function of the low gain capacitance. As an example, the curves are plotted for readout path noises of 100 and 400 µV. The blue "kT/C noise" curve shows the limit set by the kT/C noise only. Even in the absence of readout path noise the SNRt at 10 ke⁻ cannot exceed 30 dB for capacitances higher than ~300 fF. Also as an example, for a capacitance of 100 fF a read noise of 400 µV results in a very acceptable SNRt of 29 dB. While for 400 fF a challenging read noise of 100 µV results in worse SNRt of 26.5 dB and in the absence of read noise the SNRt would still fall slightly short of 29 dB.

Based on the expected LCG read noise on the product the low gain capacitance is not maximized to the highest value available on the test chip. It is chosen so that there is some margin for the SNR to degrade at higher temperature due to increased FD DSNU and still maintain 25 dB at 125°C. As the LCG read needs both low read noise and a large swing it is read with conditional analog gain of 8x and 0.5x.

Conditional gain

There are two ways to implement the conditional gain. Either there are two amplifiers processing the signal in parallel and the output of one of them is selected or there is one amplifier of which the gain can be changed while processing the sample. We chose the approach with a single amplifier for its lower power consumption.

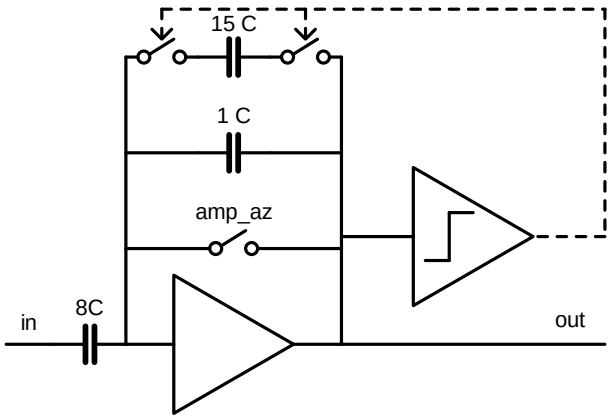

Figure 5: Schematic of the conditional gain amplifier.

Figure 5 shows a simplified schematic of the conditional gain amplifier. In the auto-zero phase of the amplifier the first pixel sample is applied to the amplifier input and both feedback capacitors are connected. This biases both capacitors correctly. The auto-zero switch is disconnected and next the 15 C capacitor is disconnected which puts the amplifier in 8x gain. After settling, this sample is converted by the ADC. Next the second pixel sample is applied and gained by 8x. If it is a small signal where the 8x gained signal does not reach the threshold, the amplifier remains in 8x gain and after settling the second sample is converted by the ADC. Subtracting both samples yields a normal CDS read. However, if the 8x gained signal does reach the threshold, the 15 C capacitor is reconnected, and the gain is dropped to 0.5x. Once more after settling the second sample is converted by the ADC. Subtracting both samples yields some imperfect CDS operation since the first sample had high gain and the second sample had low gain. This will give some increase in noise which is not much of a concern in the range where the 0.5x gain is used. However, there is charge injection from the switches that connect the 15 C capacitor. This charge injection introduces an offset in the 0.5x gain read and this offset will have mismatch and may vary with temperature and supply voltage. To mitigate potential problems the product has digital column FPN correction to correct for this charge injection. The correction is calibrated at startup and continuously updated during operation to track changes.

The conditional gain takes additional time since a decision needs to be made, but it is faster than processing the two gains sequentially and lower power than two amplifiers in parallel. The conditional gain is a key enabler for the product. It allows to save the time and power needed for the correlated multiple sampling.

Correlated multiple sampling

Correlated multiple sampling [12-14] allows reducing the read noise below what the circuits are natively capable of. Both the reset and the signal are sampled multiple times and averaged to reduce the noise. The product supports both analog and digital CMS. Analog CMS (ACMS) averages the SF and the amplifier noise while digital CMS (DCMS) additionally also averages the ADC noise. Both can be used together. However, with an analog gain of 8x the noise contribution of the ADC is very limited, and hence digital CMS is a high cost (power and speed) low benefit feature that is only useful in specific use cases like a night mode where it is acceptable to reduce the frame rate to get to the best possible low light performance. Analog CMS on the other hand is a low-cost feature. The signal is sampled multiple times on a set of capacitors which are then connected together to average the signal. It only costs the additional time to sample the signal multiple times at an interval where the noise is sufficiently uncorrelated. The input capacitance of the ADC is split in two halves that can be sampled at different times, connected together and converted once. That accounts for an ACMS of 2. There are two additional capacitors that can be sampled at different times and averaged with the ADC input capacitors to increase the ACMS to 4. In addition, a DCMS of 2 converts two samples and averages them in the digital domain. So maximally a CMS of 8 can be applied. A very preliminary measurement on the product shows a read noise of 0.6 e^- with a gain of 8x, ACMS of 2 and DCMS of 2.

A high gain (8x) naturally reduces the noise by limiting the bandwidth due to the fixed gain x bandwidth product of an amplifier. Additionally, the bandwidth can be further reduced by adding more load capacitance to the amplifier. This is an alternative use of the two ACMS sampling capacitors at the expense of a further speed reduction.

Photo diode optimization

Compared to the previous generation this pixel must handle about 4x the overflow current without blooming. This requires a stronger n-type implant for the buried channel overflow path which would lead to a reduction of the full well. This is compensated by an increased n-type doping level in the deep part of the PD so that the full well stays on par with the previous generation.

Conclusion

This paper demonstrates a single photo diode pixel with the capability of 126 dB single exposure DR. This DR is obtained by a combination of pixel and readout path improvements. For the product the DR target is slightly reduced to 124 dB to maintain an SNRt around 25 dB up to 125°C.

This combination of an excellent flicker free dynamic range and good image quality throughout the entire automotive temperature range makes this the pixel for our next generation automotive sensors.

Pixel pitch	2.1 µm
Pixel architecture	Overflow with dual in-pixel gain readout
Linear Full well	10 ke^- PD 2700 ke^- Clg (Highest on TC) 2200 ke^- Clg (Product target)
Read noise @ RT	0.8 e^- @8x gain, No CMS on TC 0.6 e^- @8x gain, ACMS=2, DCMS=2 preliminary measurement on product
Single exposure DR	126 dB, SNR1 based at RT, TC max LFW 124 dB, SNR1 based at RT, product target 131 dB, read noise based, product target
Total DR (T1+T2)	150 dB, SNR1based at RT, T1/T2=5000
Transition SNRt	28 dB at 80°C, 25 dB at 125°C

Table I. Pixel properties and performance

Figure 6: A first image from the product is grabbed in the week the paper is submitted. Product details and characterization data can hopefully be shared in the presentation at the workshop.

References

[1] O. Yadid-Pecht and E. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling", IISW 1997.

[2] J. Solhusvik et al., "A 1280x960 3.75 µm pixel CMOS imager with Triple Exposure HDR", IISW 2009.

[3] S. Velichko et al., "140 dB Dynamic Range Sub-electron Noise Floor Image Sensor", IISW 2017.

[4] M. Innocent et al., "Pixel with nested photo diodes and 120 dB single exposure dynamic range", IISW 2019.

[5] Y. Sakano et al., "A 132 dB Single-Exposure-Dynamic-Range CMOS Image Sensor with High Temperature Tolerance", ISSCC, pp. 105–107, Feb. 2020.

[6] Y. Oh et al., "A 140 dB Single-Exposure Dynamic-Range CMOS Image Sensor with In-Pixel DRAM Capacitor", IEDM 2022

[7] N. Akahane et.al. "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor", in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 851-858, April 2006.

[8] Y. Fujihara et al., "An Over 120 dB Single Exposure Wide Dynamic Range CMOS Image Sensor with Two-Stage Lateral Overflow Integration Capacitor", Electron Devices IEEE Transactions on, vol. 68, no. 1, pp. 152-157, 2021.

[9] T. Geurts et al., "A 98 dB Linear Dynamic Range, High Speed CMOS Image Sensor", IISW 2017.

[10] M. Oh et al., "3.0 µm Backside illuminated, lateral overflow, high dynamic range, LED flicker mitigation image sensor", IISW 2019.

[11] M. Innocent et al., " Automotive CMOS Image Sensor Family with 2.1µm LFM Pixel,150 dB Dynamic Range and High Temperature Stability," IISW 2023.

[12] S. Kawahito et al., "Noise Reduction Effects of Column-Parallel Correlated Multiple Sampling and Source-Follower Driving Current Switching for CMOS Image Sensors", IISW 2009.

[13] S.Kamoshita et al., "A Proposal of Analog Correlated Multiple Sampling with High Density Capacitors for Low Noise CMOS Image Sensors" in Proc. IS&T Int'l. Symp. on Electronic Imaging: Imaging Sensors and Systems, 2021, pp 92-1 - 92-6.

[14] R. Capoccia et al., "Experimental Verification of the Impact of Analog CMS on CIS Readout Noise" in Transactions on Circuits and Systems I, vol. 67, no. 3, pp. 774-784, March 2020.